Symmetric 3D Passive Components for RF ICs Application

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Abstract

This paper proposes novel 3-D symmetric RF passive components, including inductors, transformers, and baluns. Layout areas of these components are drastically reduced by means of stacked structure while the symmetry of input and output ports is also maintained. The area saving of 3-D inductor is up 70 %. The 1:1 transformer shows less than 0.1 % inductance mismatch in a 18 GHz range, and K is up to 0.87 at 17 GHz. The 3-D balun manifests less than 0.8 dB gain mismatch from 5.25GHz to 6GHz and phase error is about 4° at 5.25 GHz according to measurement results. All the components are fabricated in a 0.18 μm standard CMOS process.

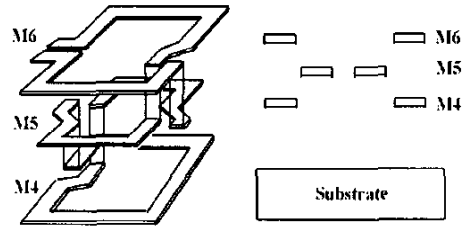
I. Introduction

With the blooming progress in CMOS technologies and VLSI circuit techniques, radio-on-a-chip (ROC) becomes a design trend for wireless devices. Among this, RF passive components play an important role in system integration, and in general have significant impacts on overall transceiver performance. Recently, several passive component architectures with improved performance have been proposed, including stacked inductors [1], miniature 3-D inductors [2], symmetric planar inductors [3], symmetric planar transformers[4], and baluns [4][5]. Also, other techniques to improve the quality factor and self-resonant frequency of the passive components have been addressed [2][6]-[8]. Conventionally, these passive components are laid out in planar spiral shape, which occupies significant chip area, especially for balun and transformer design. Although [1] and [2] proposed stacked architectures to reduce the chip area, but those miniaturized inductors are basically asymmetric.

This paper proposes novel 3-D miniaturized passive component architectures while maintaining the symmetry of input and output ports [9]. In RF ICs design, such as VCO, LNA, and mixer, fully differential architectures are preferable for they can suppress common mode noise. In these circuits, one symmetric passive component can be adopted to replace two asymmetric ones in the differential paths so as to save chip area and cost. Most important of all, by means of the miniaturized symmetric architecture, the effective inductance can be increased by inherent mutual coupling. This implies that the layout trace can be shortened to achieve the same inductance, which can benefit from smaller series resistance.

II. Symmetric 3-D Inductor

Fig 1(a) and (b) illustrate an layout example of our proposed symmetric 3-D inductors. The wire winds downwardly with right-half turn on the upper layer interleaved with the left-half turn on adjacent lower layer and vice versa. When the wire reaches the bottom layer, it winds upwardly in the counter path. In this way, the input and output port will be fully symmetric. The outer radius of loops on adjacent layers can be different to minimize mutual coupling capacitance, so as to have better self resonant frequency f_{sr}.



(a) (b)

Fig. 1.(a) Symmetric 3-D inductor structure
(b) Cross-sectional view of Fig. 1.(a)

The 3-D inductor can be characterized by the following design parameters, including the number of layers n, metal width w, inner radius r, outer radius R, and the metal spacing between adjacent wires s. Figure 2(a) shows the top view of the inductor corresponding to the design parameters. To investigate the self resonant frequency f_r of the 3-D inductors, the following assumptions are made to simplify the derivations [1][2].

(1) Ignore the parasitic capacitance between adjacent wires on the same layer.
(2) Ignore the fringing capacitance between adjacent layer with different diameter.
(3) Voltage potential is equal in half turn and is determined by averaging the voltages of the previous half turn and the next one.
(4) Voltage distribution is proportional to the length of the metal track.

For an n-layer, single turn, symmetric inductor with inner radius r and outer radius R, the ratio of perimeters l_m on each layer can be expressed as

$$l_n : l_{n-1} : l_{n-2} : l_{n-3} \ldots = 8R : 8r : 8R : 8r \ldots$$

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If n is even , we have

$$l_1 + l_2 + l_3 + l_4 ... + l_n = 4n(R+r)$$

On the contrary, if n is odd

$$l1 + l2 + l3 + l4 ... + ln = 4R(n+1)+4r(n-1)$$

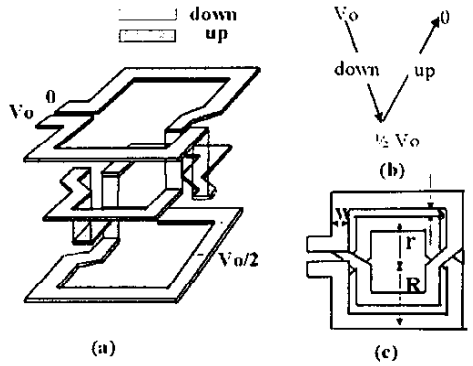


Fig. 2. (a) Layout topology (b) Voltage distribution profile (c) Top view of symmetric inductor

Let the terminal voltage of the inductor be V_o and 0, beginning and ending voltage of the *m-th* half turn metal trace be represented by $V_{mth,\ initial}$ and $V_{mth,final}$. $V_{mth,down}$ and $V_{mth,up}$ respectively represent the voltage of the m-th half turn in the downward path and upward path, the voltage distribution on each segment can be derived as

$$V_{m-th,initial} = V_o - \frac{V_o}{2}\left(\frac{l_1 + l_2 + ... + l_{n-m}}{l_1 + l_2 + l_3 + ... + l_n}\right)$$

$$V_{m-th,final} = V_o - \frac{V_o}{2}\left(\frac{l_1 + l_2 + ... + l_{n-m+1}}{l_1 + l_2 + l_3 + ... + l_n}\right)$$

$$V_{m-th,down} = \frac{1}{2}\left(V_{m-th,initial} + V_{m-th,final}\right)$$

$$= V_o - \frac{V_o}{4}\left(\frac{2(l_1 + l_2 + ... + l_{n-m}) + l_{n-m+1}}{l_1 + l_2 + l_3 + ... + l_n}\right)$$

$$V_{m-th,up} = \frac{V_o}{4}\left(\frac{2(l_1 + l_2 + ... + l_{n-m}) + l_{n-m+1}}{l_1 + l_2 + l_3 + ... + l_n}\right)$$

The voltage difference between two metal layer is

$$V_{i+2,down} - V_{i,down} = V_{i,up} - V_{i+2,up}$$

$$= \frac{V_o}{4}\left(\frac{l_{n-i-1} + 2l_{n-i} + l_{n-i+1}}{l_1 + l_2 + l_3 + ... + l_n}\right)$$

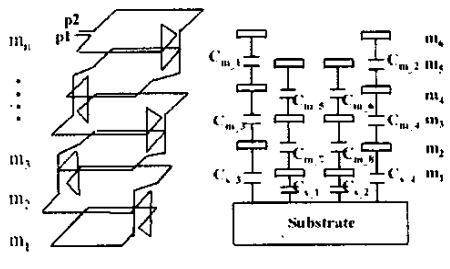


Fig. 3. (a) Single-turn 6 layer inductor (b) Parasitic capacitance of 6 layer symmetric 3-D inductor.

Fig. 3 illustrates a single turn 6-layers 3-D inductor and the distribution of parasitic capacitance. The effective capacitance C_{eq} of the 3-D inductor includes the contribution of metal-to-metal capacitance C_{mtom} and metal to substrate capacitance C_{mtosub}, which can be simulated by the total electric energy stored in the inductor [1][2]. In this topology, C_{mtosub} stems from m_1 and m_2 to substrate capacitance, and C_{mtom} is the summation of interlayer capacitances. Let $C_{mtom/\square}$ and $C_{mtosub/\square}$ be the unit capacitance . Since the total electric energy can be derived as

$$E_m = E_e = \frac{1}{2}C_{eq}V_o^2$$

$$= \frac{1}{2}\sum_{i=1}^{n-2} 2[C_{mtom/\square,i\_(i+2)} \times \frac{1}{2}l_i w \times (V_{i+2,down} - V_{i,down})^2]$$

$$+ \frac{1}{2}\sum_{i=1}^{2}[C_{mtosub/\square,i} \times \frac{1}{2}l_i w \times (V_{i,down}^2 + V_{i,up}^2)]$$

$$= \frac{1}{2}\sum_{i=1}^{n-2}[C_{mtom/\square,i\_(i+2)} \times l_i w \times (\frac{l_{n-i-1} + 2l_{n-i} + l_{n-i}}{l_1 + l_2 + ... + l_n})^2 \frac{V_o^2}{16}]$$

$$+ \frac{1}{2}\sum_{i=1}^{2}[C_{mtosub/\square,i} \times \frac{1}{2}l_i w \times (V_{i,down}^2 + V_{i,up}^2)]$$

We have

$$C_{eq} = \sum_{i=1}^{n-2}[\frac{1}{16}C_{mtom/\square,i\_(i+2)} \times l_i w \times (\frac{l_{n-i-1} + 2l_{n-i} + l_{n-i}}{l_1 + l_2 + ... + l_n})^2]$$

$$+ \sum_{i=1}^{2}[C_{mtosub/\square,i} \times \frac{1}{2}l_i w \times (\frac{V_{i,down}^2}{V_o^2} + \frac{V_{i,up}^2}{V_o^2})]$$

The equivalent inductance L_{eq} can be derived as

$$L_{eq} = \sum_{i=1}^{n} L_i + M$$

where L_i represents the inductance on each loop, and M represents the summation of mutual inductances. The self-resonant frequency can be derived as

$$f_{sr} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}}$$

Figure 4 illustrates the derived, simulated, and measured f_{sr} v.s. n with outer radius R = 45 μm in a 0.18 μm standard CMOS technology. These structures are simulated using ADS® momentum. The trends of f_{sr} by derivations, simulations, and measurements are well agreed as n is increased. According to simulation result, a 3-turn 3-D symmetric inductor has self-resonant frequency as high as 30 GHz, which is beyond the frequency range of our instrument. By offsetting diameter on adjacent loop, the parasitic capacitance is significantly reduced.

Table 1 summarizes the performance comparisons between a planar symmetric inductor and our proposed 3-D symmetric inductor by simulation. With the same inductance, the 3-D structure manifests a little better self-resonant frequency. And most important of all, the chip area can be reduced to 32 % for a 6.8 nH inductor.

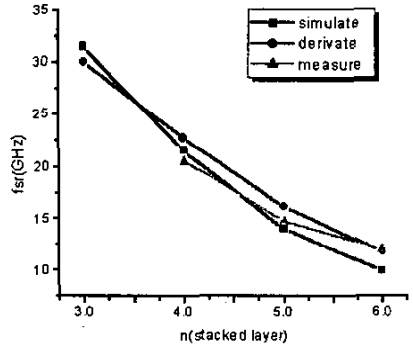


Fig. 4. f_{sr} v.s. n @ R=45 μm

Table 1 Comparison between planar symmetric and 3-D symmetric inductor

R = 55 μm	n	3	4	5	6
Planar symmetric inductor	L(nH)	1.66	2.89	4.82	6.8
	f_{sr}(GH)	19.8	11.8	8	5.8
Stacked symmetric inductor	L(nH)	1.74	2.77	4.34	6.16
	f_{sr}(GH)	20	14	9.5	6.5
$\frac{A_{stack}}{A_{planar}}$		70%	52%	40%	32%

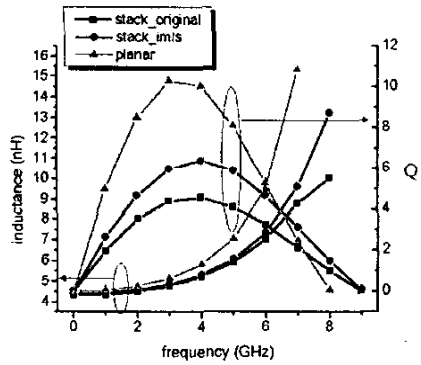


Fig. 5. Q comparison

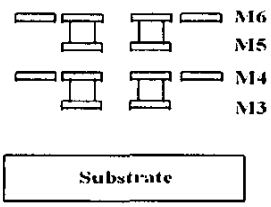


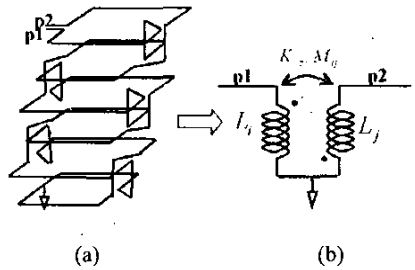
Fig. 6. Cross sectional view of improved multi level shunt (IMLS) symmetric 3-D inductor

Figure 5 shows the quality factor comparison of a planar symmetric and a 3-D symmetrical inductor by simulation. Both have the same inductance of 4.5 nH , 4 turns, w=10μm, s=1.5μm and inner radius r of 65 μm. These two inductors respectively occupy a chip area of 209 x 209 μm^2 and 163 x 163 μm^2. It reveals that the quality factor of planar inductor is better, for the planar inductor is made up of the thickest (top) metal only. The metal thickness is 2μm for the top layer metal and only 0.53μm for the bottom layer metal in this technology.

To improve the quality factor, improved multi-level shunt (IMLS) techniques can be adopted to further improve the quality factor of the proposed symmetric inductor [7]. Figure 6 shows the cross sectional view of the IMLS 3D inductor. IMLS only shunt the inner loops to compromise with parasitic capacitance and resistance. According to simulation result, IMLS can improve the quality factor by 2.

III. 3-D Transformer

A 1:1, 3-D fully symmetric transformer can be easily built up by center-tapping the middle point of a 3-D symmetric inductor to a common mode voltage or ground, as is shown in Fig 7(a). Fig 7(b) depicts the symbol view, where an inverting type transformer bridges port 1 and port 2. The magnetic coupling mainly stems from conductor loops on adjacent layers.



(a) (b)

Fig. 7.(a) 1:1 3-D transformer
(b) Inverting type transformer

The self inductance L_i, L_j ,mutual inductance M_{ij} , and coupling coefficient K can be derived as

$$L_i = \frac{\mathrm{Im}(Z(i,i))}{2\times\pi\times f} \qquad L_j = \frac{\mathrm{Im}(Z(j,j))}{2\times\pi\times f}$$

$$M_{ij} = \frac{\mathrm{Im}(Z(i,j))}{2\times\pi\times f} \qquad K = \frac{M_{ij}}{\sqrt{L_i L_j}}$$

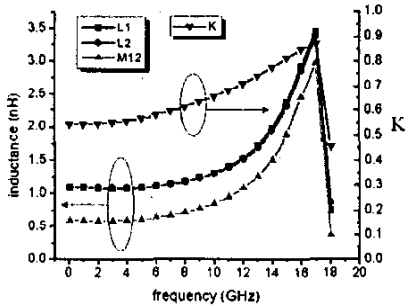


Fig. 8. L_1 , L_2 , M_{12}, K

For a $n = 6$, $w = 10\,\mu$m, $s = 1.5\,\mu$m, $R = 45\,\mu$m transformer, its self resonant frequency is about 18 GHz, inductance is 1.8 nH (L_i+M_{ij}), and coupling coefficient is 0.56 at 5 GHz by simulation. In addition, K increases along with the increment of input frequency, which is above 0.7 as input frequency extends to 12 GHz. The coupling coefficient K can be enhanced by increasing the number of turns per layer.

Ⅳ. 3-D Balun

A 3-D balun (balance to unbalance converter) can be built up by interleaving one symmetric inductor with one symmetric transformer. Figure 9 depicts the corresponding layout topology and the symbol view. The experimental results of a R= 130 μm, w=10 μm, s=1.5 μm, 3 turns/6 layer balun are shown in Fig.9. In this prototype, a single turn per layer topology is used, thus the mutual coupling mainly stems from layer to layer magnetic coupling. The insertion loss is less than 5 dB around the 5 GHz band of interests, which can be further improved by increasing the number of loops per layer. Figure 10 (a) and (b) respectively show the measurement result of gain and phase response. The 3-D balun manifests less than 0.8 dB gain mismatch from 5.25GHz to 6GHz and phase error is about 4° at 5.25 GHz frequency band of interests.

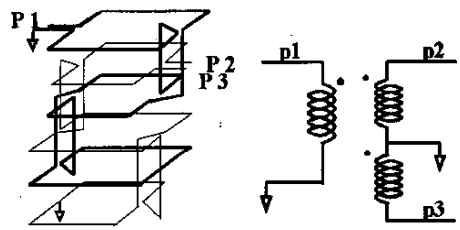


Fig. 9. Symmetric stacked balun

V.Conclusion:

This paper presents novel miniaturized 3-D symmetric passive components for RF ICs applications. Compared to conventional symmetrical planar architecture, the 3-D inductors manifest comparable self-resonant frequency and quality factor with layout area of less than 32% along with the increment of inductance. In addition, 3-D symmetric transformer and balun can be easily derived from the miniaturized symmetric inductor. These component shows wide band gain and phase match.

Acknowledgement

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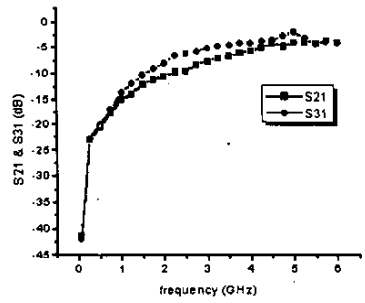
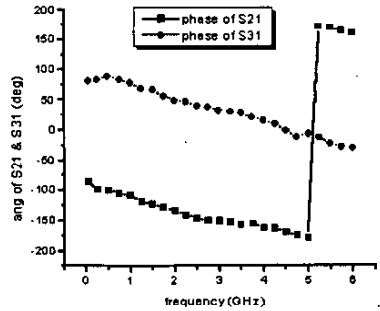
References:

1."Stacked Inductors and Transformers in CMOS Technology, " Alireza Zolfaghari, Andrew Chan, Behzad Razavi, IEEE JSSC vol.36.NO.4. April 2001 pp.620-628



(a) Gain response



(b) Phase response

Fig. 10. 3D balun measurement result (a) S21 and S31 gain response (b) S21 and S31 phase response

2."Miniature 3-D Inductors in Standard CMOS Process," Chih-Chun Tang, Chia-Hsin Wu, Shen-Iuan Liu,IEEE JSSC vol.37.NO.4, April 2002 pp.471-480

3."Differentially Driven Symmetric Microstrip Inductors, " Mina Danesh, John R. Long, IEEE Trans. Microwave Theory Tech.,vol.50,no. 1, January 2002.

4."Monolithic Transformers for Silicon RF IC Design, " John R.Long, IEEE JSSC vol.35.NO.9.September 2000 pp1368-1382

5."Design and Modeling of Compact On-Chip Transformer/Balun Using Multi-Level Metal Winding for RF Integrated Circuit ," Tao Liang, John Gillis, Dawn Wang, Paul Cooper, IEEE RFIC Symposium 2001, pp117-120

6."On-chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," C.Patrick Yue, S. Simon Wong, IEEE JSSC vol. 33, NO.5, May 1998 pp743-752

7."Microwave inductors and capacitors in standard multilevel interconnect silicon technology," J. N. Burghartz, M, Soyuer, K. A. Jenkins, IEEE Trans. Microwave Theory Tech., vol. 44,no 1, Jan 1996 pp100-104

8."A Q-factor enhancement technique for MMIC inductors," Mina Danesh, John R. Long, R. A. Hadaway, D. L. Harame, IEEE RFIC Symposium 1998 pp217-220

9. W.-Z. Chen and W.-H. Chen, "3-D symmetric RF passive components," U.S. and R.O.C. patent pending.